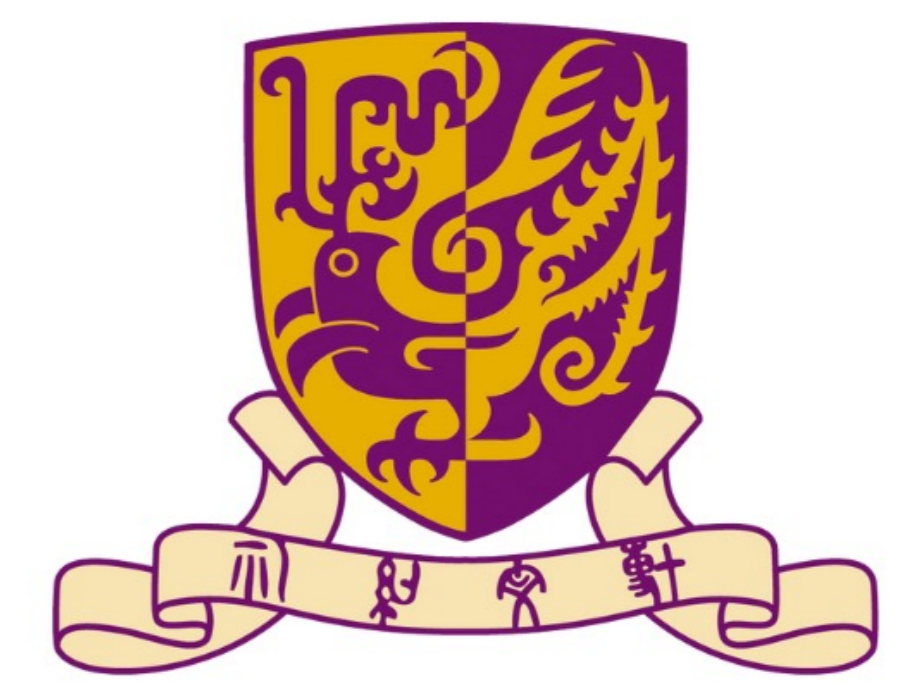


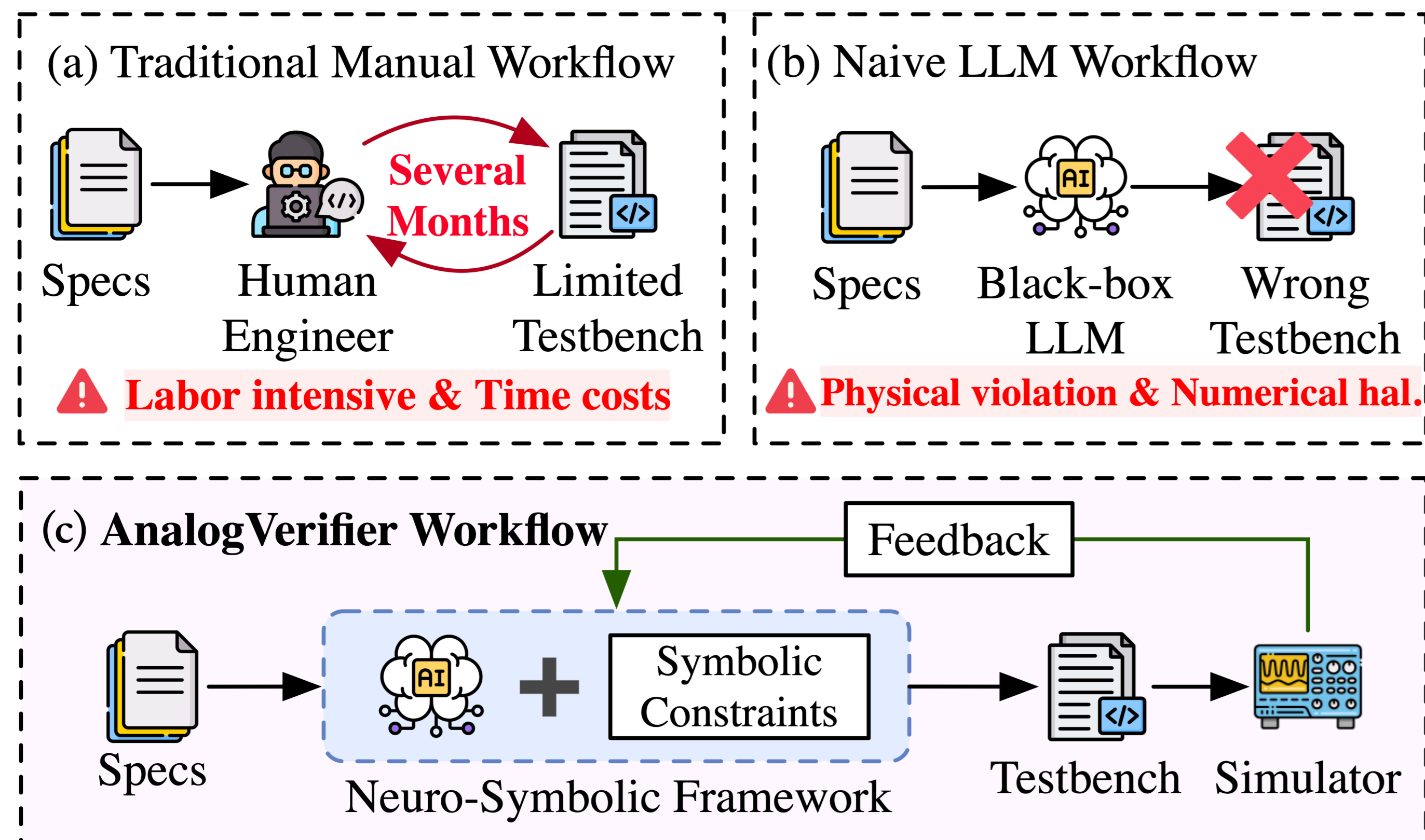
AnalogVerifier: A Neuro-Symbolic Framework for Analog Circuit Verification

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Background & Motivation



- Verification consumes 50-70% of analog design effort
- Testbench often requires months of manual engineering.
- Naive LLM generation is unreliable for safety-critical analog verification.

Challenges & Main Contributions

Semantic Dispersion

Physical Dependency

Numerical Hallucination

Neuro-Symbolic Framework

Context-Aware Task Serialization

Transforms unstructured specs into atomic verification tasks.

Graph-Symbolic Scheduling

Constructing a Port Dependency Graph (PDG) that explicitly encodes physical precedence relations

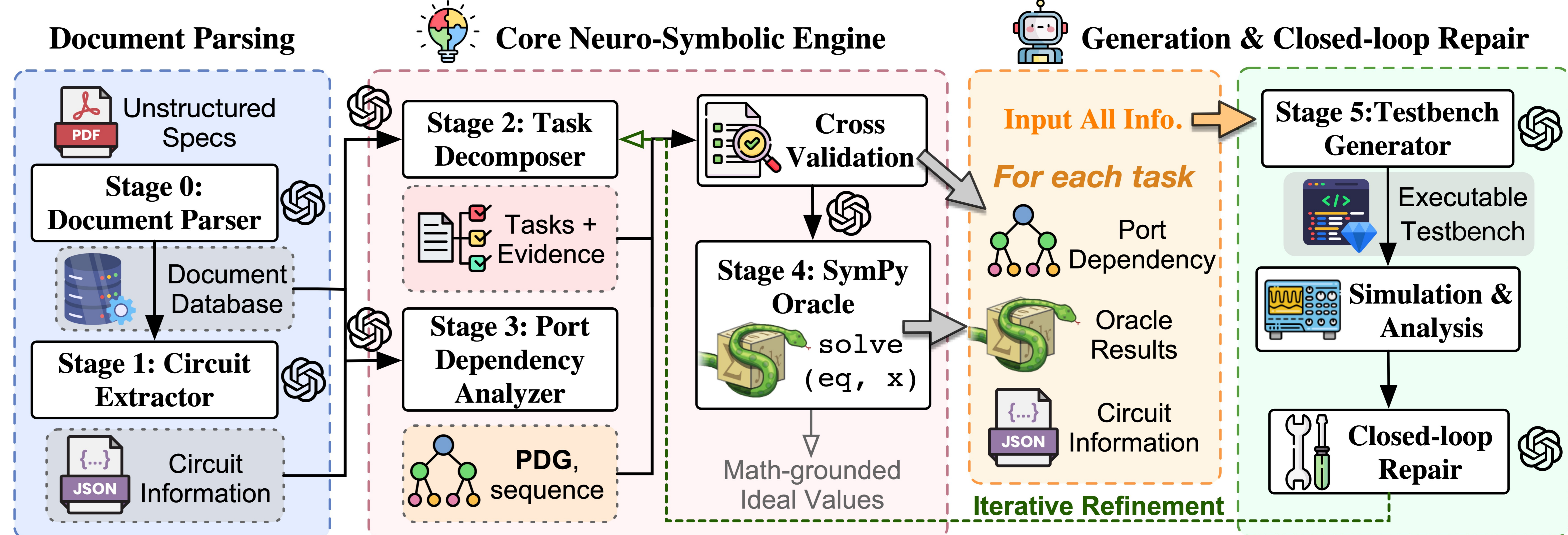
Numerical-Symbolic Grounding

The LLM translates specification requirements into symbolic expressions; the SymPy-based oracle performs exact arithmetic with interval propagation,

Closed-loop Repair

Iteratively fixes errors using simulation feedback

AnalogVerifier Framework



- 1 Context-Aware Task Serialization: Transforms unstructured specs into atomic constraints via an agentic frontend (Stages 0-2).
- 2 Dual-Stream Symbolic Enforcement: Enforces physical correctness via Graph-Symbolic Scheduling (for temporal causality) and Numerical-Symbolic Grounding (for precise numerical assertions) (Stages 3-4).
- 3 Testbench Generation & Repair: Synthesizes code from verified artifacts and iteratively corrects errors via closed-loop simulation feedback (Stage 5).

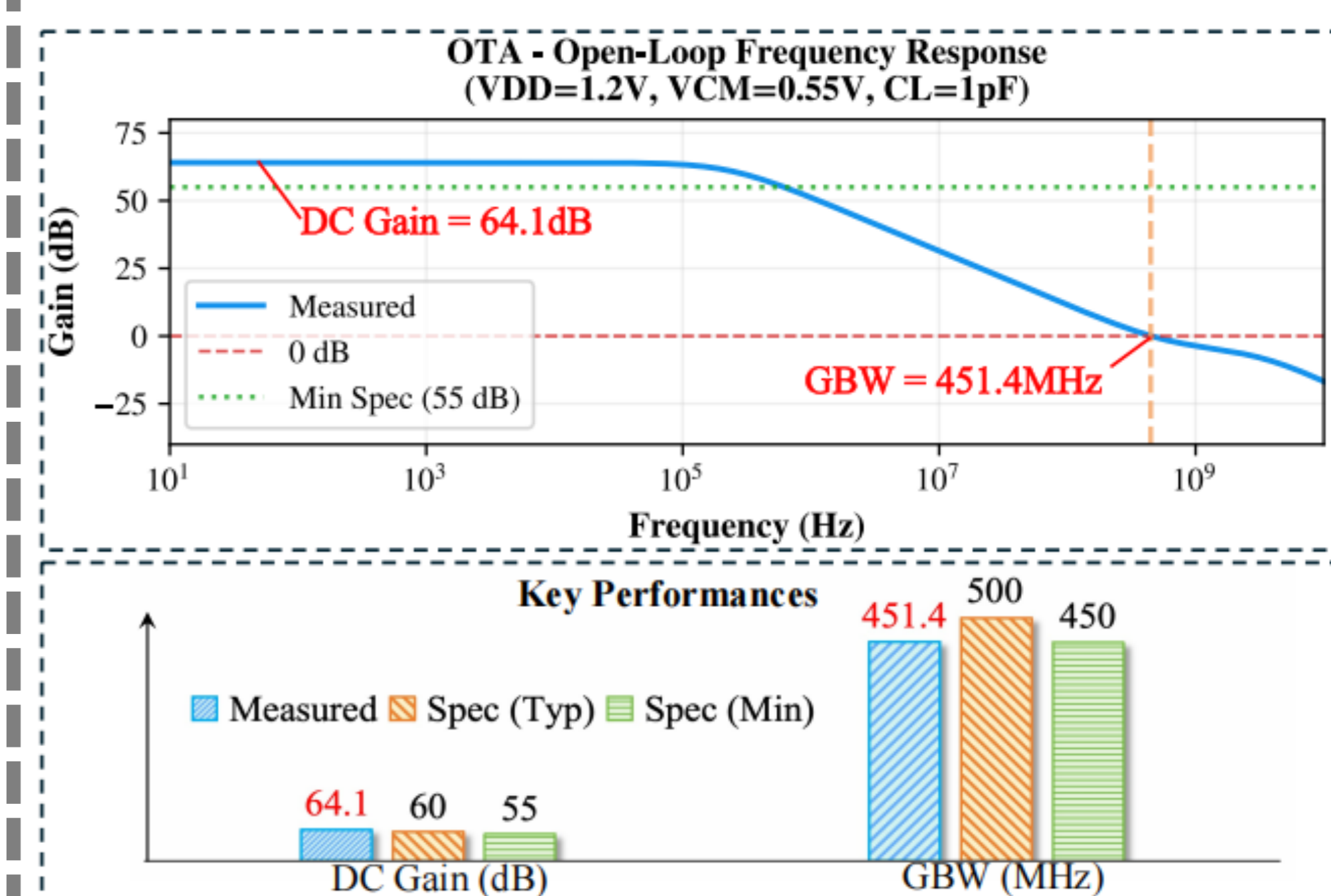
Experimental Results

- Evaluation on five industrial analog circuits demonstrates that AnalogVerifier achieves **82.3%–100% functional pass rate**, establishing a new paradigm for reliable, automated analog verification.

Circuit	Model	w/o AnalogVerifier				AnalogVerifier w/o Repair				AnalogVerifier (Ours)			
		#Task	Rec.	Prec.	Pass	#Task	Rec.	Prec.	Pass	#Task	Rec.	Prec.	Pass
OTA	GPT-5.1	9	18.8	33.3	–	23	62.5	52.6	30.4	23	62.5	52.6	91.3
	Claude-Sonnet-4.5	11	31.2	45.5	9.1	29	87.5	63.6	37.9	29	87.5	63.6	93.1
	Claude-Haiku-4.5	14	37.5	42.9	–	39	87.5	43.8	33.3	39	87.5	43.8	92.3
DCDC	GPT-5.1	15	16.7	40.0	6.7	50	69.4	54.3	90.0	50	69.4	54.3	100.0
	Claude-Sonnet-4.5	19	25.0	47.4	–	58	88.9	61.5	87.9	58	88.9	61.5	98.3
	Claude-Haiku-4.5	24	27.8	41.7	4.2	84	88.9	42.7	69.0	84	88.9	42.7	96.4
HSC	GPT-5.1	13	9.5	30.8	–	44	47.6	46.5	61.4	44	47.6	46.5	95.5
	Claude-Sonnet-4.5	20	19.0	40.0	–	81	85.7	48.0	50.6	81	85.7	48.0	95.1
	Claude-Haiku-4.5	27	26.2	40.7	3.7	118	95.2	38.8	28.8	118	95.2	38.8	91.5
RO	GPT-5.1	10	6.5	20.0	–	27	16.1	22.7	40.7	27	16.1	22.7	92.6
	Claude-Sonnet-4.5	17	22.6	41.2	5.9	74	93.5	50.0	73.0	74	93.5	50.0	95.9
	Claude-Haiku-4.5	22	29.0	40.9	–	87	100.0	41.9	57.5	87	100.0	41.9	95.4
SDC	GPT-5.1	14	12.5	28.6	–	96	43.8	36.8	42.7	96	43.8	36.8	82.3
	Claude-Sonnet-4.5	18	21.9	38.9	5.6	91	87.5	52.8	59.3	91	87.5	52.8	92.3
	Claude-Haiku-4.5	24	28.1	37.5	–	117	100.0	40.0	54.7	117	100.0	40.0	93.2

Notes: #Task = number of extracted test tasks; Rec. = task recall (%), coverage of human-annotated reliable reference tasks; Prec. = task precision (%), proportion of extracted tasks matching reliable references; **Pass = functional validation pass rate (%)**. “–” indicates simulation failure. Best pass rates per row are in **bold**.

Case Study: OTA Verification



OTA open-loop frequency response and key performance metrics. Top: Bode plot showing DC gain of 64.1 dB and GBW of 451.4 MHz. Bottom: Comparison between measured values and specification targets on key performance (DC Gain and GBW).